كلية التقنية التقنية الالكترونية - طرابلس اسم الطالب ..... رقم الطالب .....

to the following table, choose from item 2 that matches item 1. (14x0.5=7 marks)

	Item 1	Item 2	A
1	Interface	transfers data between RAM and I/O without having to go through CPU	
2	The 8086 processor	can supports 256 different interrupts	
3	PIC 8259	Can work with other CPU in the same system	
4	If interrupt occurs	1 chip contains group of µchips that are designed to work with 1 or more related functions	
5	Multi Core processor	a controller used to manage the timing between computer devices	
6	8086 in maximum mode	More than 1 processor in a single chip	
7	PIT-8253/8254	Input/output ports are treated by CPU as RAM locations	
8	PPI 8255	A data structure with FILO data access mechanism	
9	Stack	Auto set to 1 if arithmetic operation result <1	
10	Sign Flag, SF	Controls the interface between CPU and I/O ports	
11	Chipset	Automatically CPU pushes the flags and the next instruction address in the stack	
12	DMA controller 8257	Controls the interrupts priority	
13	Memory mapped I/O	electronic circuits that make the computer compatible with the peripherals	
14	Instruction cycle	programmable interval timer controller	

Q5- Choose the right answer (20x0.5 = 10 marks)

3-1. CPU architecture using microprogramming makes it
a) more complex architecture b)more expensive c)more efficient d) more integrated e) all f) non of all

3-2. A µP is capable of addressing a 1M Bytes of memory if it supports
a) 8 bit data bus and 20 bit address bus. b) 16 bit data bus and 25 bit address bus.
c) 20bit address bus and 8 bit data bus. d)16 bits control bus and 24 bit address bus and 20 bits data bus

3-3. Program counter is incremented automatically
a) before finishing of execution of current instruction b) after finishing of execution of current instruction
c) after fetching of current instruction d)at same time e)All f) none of the all

3-4. in 8086 the physical address is computed by a)BIU b) EU c) ALU d)RAM

3-5. Segmentation is applied to a) registers b) RAM c)ROM d) ALU e)data bus f)CPU g)Address bus h)DMA i)all

3-6. In segmentation, segments
a) should be same size b) code segment must be larger d)could be same or different size
d) data segment must be larger e)stack segment must be the largest f) none of all

3-7. Program Counter (PC) represents
a)physical Address In ALU b)Effective Address in RAM c) physical Address in DMA
d)physical Address in RAM e)Effective Address in ALU f)Effective address In stack

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3-8. the most flexible addressing mode that can be changed in run time is
a) register b)immediate c)indirect register e)indirect memory

3-9. The way of how the addressing of source and destination in an instruction is called
a) data mode b)addressing mode d)bus mode e)execution mode

3-10. In an assembly instruction format, the first fields is the a) source of data b)destination of data c)operation code
d)Segment name e)directives f) immediate data g) data addressing mode h)non of all

3-11. Which of the flowing instruction is the fastest? a) add cx,dx b) add bx,cx c) add ax,bx d) add bx,ax e)add ax,ax

3-12. Which of the following causes RAM access if it is used a) indirect register addressing mode b) register addressing mode
c) Immediate addressing mode d)All e) not of all

3-13. Instruction pipelining system introduces
a) faster single instruction execution- b)faster over all process execution
c)faster hardware access d) faster program counter e) all f) not of all

3-14. In 8086,which of the following registers which is used as loop counter?
a) CX b) BX c) AX d)DX e)DI f)DS

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3-15. In 8086 supports maximum segment size of _____ locations (bytes) of memory
(20bytes -64 bytes- 4k--8k--16k--20K--32k--64k--128k--256k--512k--1M--2M---1G--2G--20G)

3-16. micro programming is used to design
a)control unit b)ALU c)Registers d) RAM e) stack f)All g) none of all

3-17. In assembly language programming, directives are used to tell
a) user what to b) programmer what to do c) processor what to do
d) assembler what to do e)all f) none of all

3-18. PPI 8255 is used as interface controller to control a) interrupts b) I/O ports d) clock timing e) RAM

3-19. PIT 8253/8254
a) generates peripheral clock signal b)can be programmed to give the desired timing and delay
c) used as Sync/Async. transmitter and receiver d)control serial transmission e)all

3-20. DMA controller: used to transfer data (_____)without having to go through CPU
a) between RAM and RAM or I/O and RAM b)between ALU and RAM
c) between CPU and RAM d) between I/O ports and CPU e)all

GOOD LUCK

Q.6. Assume that a CPU uses instructions pipelining for three instructions, each instruction segmented to five stages as:

1. Fetch (F)
2. Decode (D
3. Execute (E)
4. Read (R),
5. Write (W)

By assuming that each stage takes 1 Clock Cycle(CC), 1CC = 2ns, latency = 0 and all instructions are completely independent, do the following: **(Total 7 marks)**

(a)use sketching to show pipelining mechanism) **(1marks)**

b) calculate the time needed to finish the overall process of execution of the 3 instructions using
   (i) sequential **(1 marks)**
   (ii) pipelining **(1 marks)**

(c) calculate the process throughput (instruction/s) in both cases, sequential and pipelining - **(1 mark)**

(d) using your results calculate the speedup in this process. **(1 mark)**

(e)by assuming CC=2ns, latency = 0 and all instructions are completely independent, if process has 1000 instructions each of 5 stages

(i) if the time needed to finish a process of *n* instructions each of *k* stages is ***(k+(n-1) CC***, calculate the time needed to finish a process of *1000* pipelined instructions each of 5 stages **(1 mark)**

(ii) calculate the time of 1000 sequential instruction **(1 mark)**

Q.7- briefly answer the following **(7 marks)**

a) What 8086 minimum and maximum modes mean?, **(1marks)**

b) Referring to 8086 pins and signals shown in Fig.1, list down the signals if maximum mode is used showing corresponding signals if minimum mode is used (use table below) **(2marks)**

Pin number	Min Mode signal	Max Mode signal

c) State the name and function of each chip shown in Fig.2 **(4 marks)**

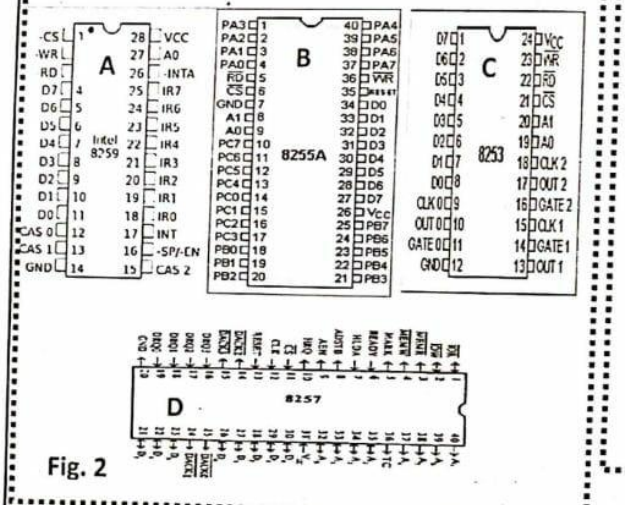

Fig. 2

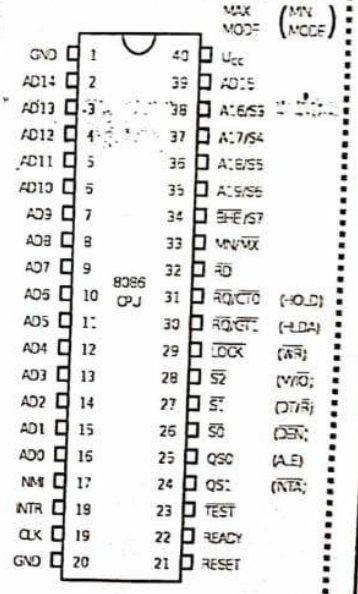

Fig. 1

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المادة: انظمة CE232-CE223 (امتحان نهائي) القسم: حاسب+تحكم

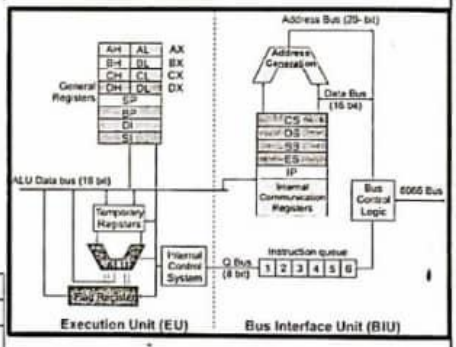
استاذ المادة: مصطفى دومة-- التاريخ: السبت 28-07-2018

Question - (Marks)	Q1-(4)	Q2-(12)	Q3-(4)	Q4-(7)	Q5-(10)	Q6-(7)	Q7-(7)	Q8-(2.5)	Q9-(3.5)	Q10-(3)	Total-(60)
Answer- (Marks)											

is ⑩ Questions in ④ Pages. ⑦ (②HOURS) Σ Marks=60

Q1-Put (✓) for right answer and (×) for wrong answer **(8x0.5=4marks)**

1-1. Buffers are needed if any connected devices are working at different speed ( )
1-2. DMA makes the computer more efficient for transferring a huge of data between I/O and RAM ( )
1-3. More Data lines in CPU increases the throughput of computer system ( )
1-4. Clock generator 8284 is used to bring down the CPU frequency to the desired level ( )
1-5. in 8086 Zero Flag ZF is used to detect errors ( )
1-6. Intel 4004 is the 1st CPU in single chip introduced to the market ( )
1-7. Parallel transmission is very high speed and cost ( )
1-8. Parallel transmission is mostly used for long distance ( )



Q2. a) In the following 2 tables choose the right answer (5marks)

Item	8085	8086
Data bus bits	8-16--20-	8-16--20-
pipelining	YES-NO	YES-NO
Memory Segmentation support	YES--NO	YES--NO
Max memory space	1M---64k	1M---64k
Maximum mode	YES--NO	YES--NO

Property	CISC	RISC
Clock Cycle(s) per instruction	1 / More than 1	1 / More than 1
microprogramming	YES -/ NO	YES -/ NO
Complexity	Higher / Lower	Higher / Lower
Number of registers	More / Less	More / Less
Code density	Higher / Lower	Higher / Lower
examples	µC CPU / GP CPU	µC CPU / GP CPU

GP => general purpose

CE232

Q2 b) fill the column 2 of the following table as related to column 1 **(7 marks)**

Registers category	Register(s) names
General purpose register(s)	
Computer status register(s)	
Pointers or offsets or index registers	
Segments registers	
EU registers	
BIU registers	

Q3-Fill the spaces in the following sentences **(14x0.25=4 marks)**

2-1. An instruction cycle is as: An instruction located in (_____) segment at memory location address pointed by (_____) is fetched by (_____) unit, then instructions ordered in a queue which can hold up to (___) bytes of instructions, then they passed to (_____) unit for decoding then (_____), If the result of execution needed to save in memory, it will pass to (____) unit to transfer it to memory

2-2. a) The first CPU introduced to market by Intel is ( ) and it is a (__) bits CPU
b) The last CPU introduced by Intel is ( ). and it is a (____) bits CPU
c) Your Mobile or laptop CPU is ( ) and it is a ( ) bits CPU

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2-3. The code segments offset (effective address) is represented by the value in (_____) register. If this offset = (A63F)h and CS register contents is (F49C)h then the physical address will be ( )